COL215 Mini-Project Report-3

CRC-CCITT Computation

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**Detailed description of the overall design**

The BRAM unit stores new inputs every time push button 1 button is pressed. Push button 2 is used for reseting. Calculation is triggered when either of push button 3, push button 4, push button 5 is pressed. Push button 4 & push button 5 modify input before calculation to showcase CRC of erroneous input. The CRC calculation is done in the same way as defined previously. Addresses of input present in BRAM cell corresponding to the calculation of push button 3, push button 4 and push button 5 are stored in separate registers and will be displayed when calculation is done. After FSM sends done signal CRC is displayed on the SSD.

**Description of the major subsystems/components and interconnecting signals**

Since the problem statement changed signals added

**BRAM component related signals**

din – input to write in BRAM

dout – output from BRAM

enable – enable signal for BRAM

reset – reset register in BRAM to 0

wen - “1111” to use BRAM in write mode and “0000” for read

**FSM unit**

pb1 = To load the 16-bit inputs in a BRAM (for n = 10).

pb2 = To reset the CRC computation and reset the checksum to the seed value.

pb3 = To start the CRC computation with no error introduced.

pb4 = To start the CRC computation with error introduced in the 5th word at

7th bit.

pb5 = To start the CRC computation with error introduced in the 3th word at

12th bit.

counter = 0 to 31 to count xor operations

done = 0 or 1 indicating computation done or not

polynomial = crc polynomial

state = 1 or 2 or 3

err1 = input with error of type 1

err2 = input with error of type 1

**Status of coding**

After the modification in problem statement we are using BRAM with our previously written code which was for 1 input. Now BRAM stores multiple inputs for which CRC is calculated

**Status of testing**

We haven’t tested FSM combined with BRAM unit yet as something are yet unclear regarding new problem statement.